What Is Claimed Is:

Sub A1

1. A digital broadcast receiving tuner, wherein the digital broadcast recording tuner has an insulating board provided with a wiring pattern each on both surfaces thereof, and wherein on one surface of the insulating board there is formed a first tuner while on the other surface thereof there is formed a second tuner.

2. The digital broadcast receiving tuner according to Claim 1, wherein the insulating board is structured of a stacked multi-layer board, and the first and second tuners are electrically shielded from each other by a grounding conductor layer provided within the multi-layer board.

3. The digital broadcast receiving tuner according to Claim 2, wherein the first and second tuners have a high-frequency unit and a demodulation unit respectively, and wherein the high-frequency unit of the first tuner and the demodulation unit of the second tuner, and the demodulation unit of the first tuner and the high-frequency unit of the second tuner are arranged at a position opposite to each other with the multi-layer board interposed therebetween respectively.

4. The digital broadcast receiving tuner according to Claim 3, wherein the multi-layer board is formed of at least three layers, wherein between lamination layers, there are provided at least the two grounding conductor layers, wherein in a region in which the high-frequency unit is provided, the grounding conductor layers arranged near the high-frequency

unit are provided with deletion units; and wherein in a range in which the demodulation unit is provided, the grounding conductor layers arranged near the demodulation unit are provided with a first remainder to thereby increase a facing distance between the wiring pattern of the high-frequency unit and the first remainder.

5. The digital broadcast receiving tuner according to Claim 4, wherein the high-frequency unit has an IC component having a direct conversion unit including an oscillator and a mixer, and the grounding conductor layer arranged near the high-frequency unit is provided with a second remainder to oppose a lower portion of the IC component.

add A12